2023년 2월 14일(화), 10:55-12:40
Room C (사파이어 I, 5층)

A. Interconnect & Package 분과
[TC2-A] Advanced Package

좌장: 김병준 교수(한국공학대학교), 정성엽 박사(삼성전자)

TC2-A-1 **10:55-11:10**	**Improvement of T&R Side Defect Screen-ability based on Deep Learning** Myeong-Jae Jin, Tae-Woo Kim, Hwee-Jo Jeong, Kwon-Whan Han, and Woong-Sun Lee *WLP Technology, SK Hynix*
TC2-A-2 **11:10-11:25**	**패키지 방열 설계를 위한 열-전기 해석의 Co-Simulation** Bongmin Jeong[1,2], Aesun Oh[2], Gawon Lee[1], and Hyuncheol Bae[2,3] *[1]Chungnam National University, [2]ETRI, [3]University of Science and Technology (UST)*
TC2-A-3 **11:25-11:40**	**Effect of Cu Pad Dimension on Cu/SiCN Hybrid Bonding Process: A Finite Element Analysis Study** So-Yeon Park[1], Cha-Hee Kim,[1] Gwang-Sik Oh[2], Young Su Yun[3], Jiho Kang[3], Sarah Eunkyung Kim[2], and Won-Jun Lee[1] *[1]Department of Nanotechnology and Advanced Materials Engineering, Sejong University, [2]Department of Semiconductor Engineering, Seoul National University of Science and Technology, [3]SK Hynix*
TC2-A-4 **11:40-12:10** **[초청]**	**SMART Metallization for Reliable Neuromorphic Edge Computing** Hanwool Yeon *GIST*
TC2-A-5 **12:10-12:40** **[초청]**	**The Challenges of Molded Underfill Materials for High Bandwidth Memory (HBM)** Kyu Won Lee, Hyoung Chul Kwon, and Seung-Hee Jo *SK Hynix*