2023년 2월 15일(수), 10:45-12:30
Room L (다이아몬드 II, 6층)

G. Device & Process Modeling, Simulation and Reliability 분과
[WL2-G] Characterization and Compact Model

좌장: 우지용 교수(경북대학교), 김성호 교수(세종대학교)

WL2-G-1 **10:45-11:00**	**TCAD Analysis of Low Resistance Ohmic Contacts to 2DEG Structures** Sethu Merin George, I.G Lee, H.B Jo, and Dae-Hyun Kim *School of Electronics Engineering, Kyungpook National University*
WL2-G-2 **11:00-11:15**	**Modeling and Characterization of Contact and Spreading Resistances in Vertical 3D Silicon FET with Asymmetric Structure** Jae Wook Yoo[1], Ji-Man Yoo[2], Hong Seung Lee[1], Hyeon Jun Song[1], Seongbin Lim[1], Jo-Hak Jung[1], Kihyun Kim[1], Keun Heo[1], Yang-Kyu Choi[2], and Hagyoul Bae[1] *[1]Jeonbuk National University, [2]KAIST*
WL2-G-3 **11:15-11:30**	**On the Universality of Drain-induced-barrier-lowering in FETs** Su-Min Choi[1], Wan-Soo Park[1], Ji-Hoon Yoo[1], Hyo-Jin Kim[1], Hyuk-Min Kwon[2], Takuya Tsutsumi[3], Hiroki Sugiyama[3], Hideaki Matsuzaki[3], Jang-Kyoo Shin[1], Jae-Hak Lee[1], and Dae-Hyun Kim[1] *[1]Kyungpook National University, [2]Polytechnics, [3]NTT Co.*
WL2-G-4 **11:30-11:45**	**Automatic Prediction of MOSFET Threshold Voltage Using Machine Learning Algorithm** DongGeun Park[1], Seoyeon Choi[1], Min Jung Kim[1], Seain Bang[1], Jungchun Kim[1], Seunghee Jin[1], Ki Seok Huh[1], Donghyun Kim[1], Jerome Mitard[2], Chul Han[1], and Jae Woo Lee[1] *[1]Department of Electronics and Information Engineering, Korea University, [2]Imec*
WL2-G-5 **11:45-12:00**	**Extraction Technique for Characteristic Parameters in Si MOSFETs through the Dual Sweep Current-to-Transconductance Ratio** Ju Young Park, Han Bin Yoo, Haesung Kim, Ji Hee Ryu, Seung Hyeop Han, Jong-Ho Bae, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim *Kookmin University*
WL2-G-6 **12:00-12:15**	**Strategies for Generating Data-efficient Neural Compact Model Using Measured MOSFET Data** Kyung Jin Rim[1], Kyungmin Kim[1], Haesung Kim[2], Ha Neul Lee[2], Junseong Park[2], Dong Myong Kim[2], Jong-Ho Bae[2], Chanwoo Park[1], and Soogine Chong[1] *[1]Alsemy Inc., [2]School of Electrical Engineering, Kookmin University*
WL2-G-7 **12:15-12:30**	**Development of In-House Compact Model for Multigate MOSFETs Using the Verilog-A** Seong-Min Han, Kwang-Woon Lee, and Sung-Min Hong *School of Electrical Engineering and Computer Science, GIST*